

The diagram illustrates a digital signal processor (DSP) system architecture. The central component is the DSP (10), which is connected to several other modules:

- ROM (12)**: Read-Only Memory, connected to the DSP via multiple bidirectional lines.
- RAM (14)**: Random Access Memory, connected to the DSP via multiple bidirectional lines.
- Logic interface (26)**: Connected to the DSP's interrupt input (*Int*) and provides control signals (*PRAB*, *PRDB*, *DRAB*, *DRDB*, *DWAB*, *DWDB*) to the memory units.
- Scan-path interface (18)**: Connected to the DSP and the switching circuit.
- Switching circuit**: Receives inputs from the scan-path interface and outputs to the host interface and universal I/O.
- Host interface**: Facilitates communication between the DSP and external systems.
- Universally used I/O**: Provides general-purpose input/output capabilities.

Additional components and connections include:

- LAB**, **LDB**, and **LCB**: Control or status signals originating from the logic interface.
- Output lines (16, 20, 22, 24)**: Represented by arrows pointing away from the system, indicating data or control output paths.

19

24

To the scan-path interface circuit (18)

Gate circuit

36

To the terminal pin for the emulation

20

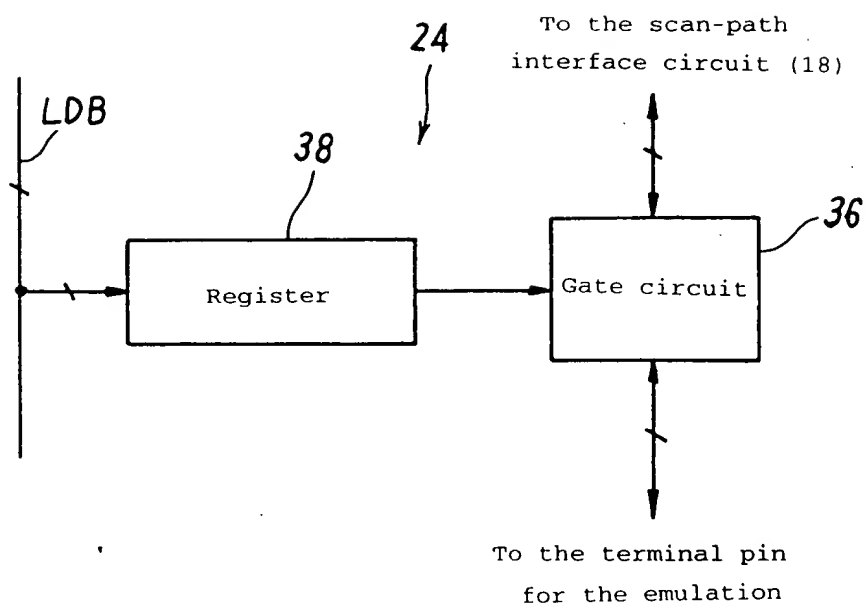


FIG. 3

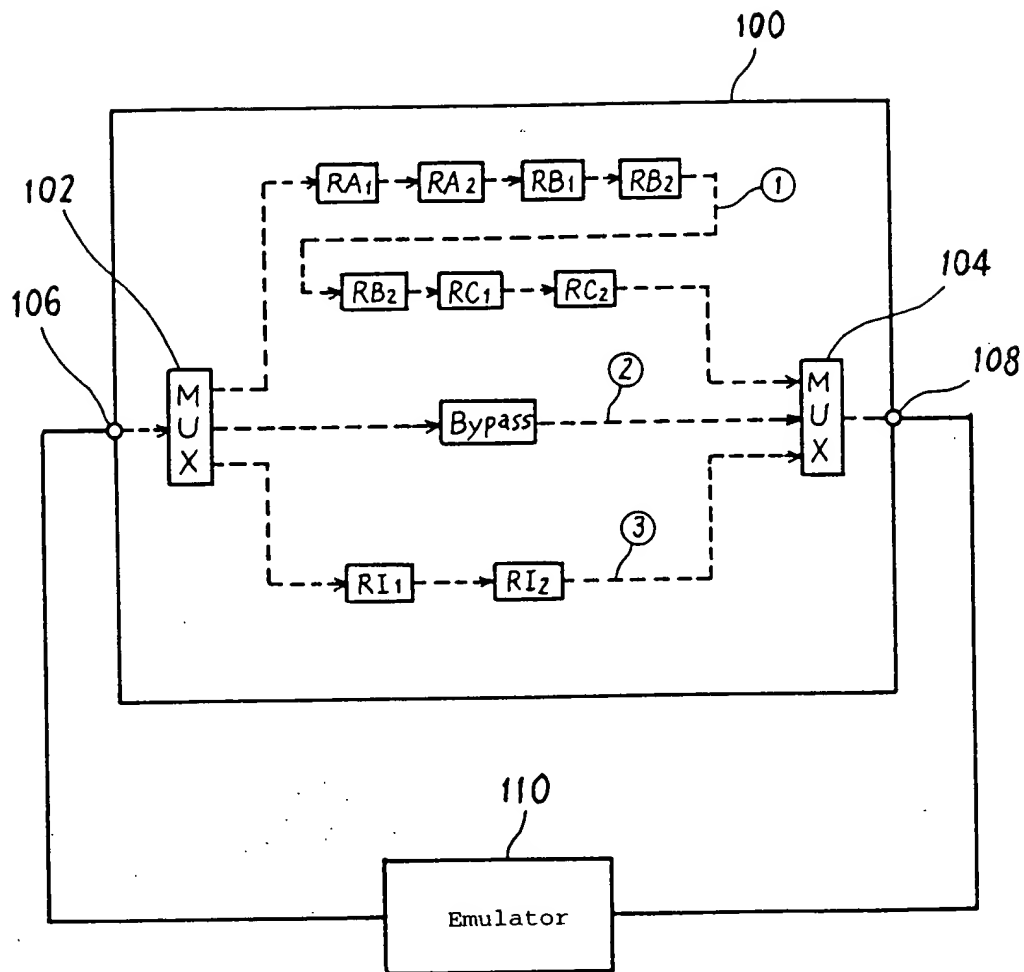


FIG. 4